Amendments to the Drawings:

The attached drawings sheets include changes to FIGS. 6A and 6B:

- In FIG. 6A and 6B (replacement drawing sheets) the reference number --701– has been added to identify the bottom face of the integrated circuit 702 as described in the specification, paragraph **[0056]**.

Attachments: Annotated Drawing Sheets showing changes to FIGS. 6A and 6B (2 pages);
Copy of Replacement Drawing Sheets (2 pages); and
Replacement Drawing Sheets (2 pages)

Remarks/Arguments

Applicants acknowledge with appreciation that Claims 21-23, 25 and 26 were indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants further acknowledge with appreciation the Examiner's availability to participate in a telephone interview held January 27, 2006 with the agent whose signature appears below, Victoria A. Poissant, and the inventor, Tom Xiaohai He. During the interview, some proposed amendments to independent Claim 15 were discussed to overcome the rejections presented in the Office Action mailed October 28, 2005. No agreement was reached during the interview, but the Examiner agreed to consider the proposed amendments as currently presented in the "**Amendments to and Listing of Claims**."

By way of the present amendment, Applicants have canceled Claims 1-14 and 28-32; amended Claims 15-17, 21-23, and 26. Thirteen (13) claims remain pending in the application: Claims 15-27, of which Claim 15 is independent. Applicants respectfully request reconsideration of the pending claims, in view of the amendments above and comments below.

Specification and Drawings

The Examiner requested that a new title be provided that is clearly indicative of the invention to which the claims are directed. Applicants have amended the title adopting the Examiner's suggestion. The title has been changed to: --METHOD OF MAKING AN ELECTRONIC MODULE --.

Applicants have also herein amended the specification, specifically paragraph **[0056]** to include reference to the bottom face 701 of the integrated circuit 206. The bottom face of the integrated circuit is shown in FIGS. 6A and 6B. Reference number --701-- has been added to FIGS. 6A and 6B to identify the bottom face. No new matter has been introduced by way of these amendments. Replacement drawing sheets which include FIGS. 6A and 6B are submitted herewith.

Claim Rejections - 35 U.S.C. § 102(e)

The Examiner rejected Claims 15, 19, 20, and 24 under 35 U.S.C. § 102(e), as being anticipated by Bates et al., U.S. Patent No. 6,635,958.

Anticipation requires that each and every element set forth in the claim be found in a single prior art reference. **MPEP §2131**. As now amended, Independent Claim 15 contains two elements which are not found or taught in Bates et al. The elements, "*providing an integrated circuit, wherein the integrated circuit comprises a top face and a bottom face*" and the element "*creating a multi-layer surface on the top face of the integrated circuit*", are not shown or taught in the Bates et al. reference.

The Bates et al. reference teaches the construction of ceramic packages for enclosing or housing electronic devices. One embodiment of the ceramic package 10, as taught by Bates and shown in FIGS. 1-3, is made from a core or base 12 with a first layer or base layer 20 of ceramic material, which can be composed of one or more layers of ceramic tape, and is positioned on the core 12. See Col. 4, lines 37-38. A second or upper ceramic layer 30 is disposed over the first layer 20. See Col. 4, lines 57-58. The ceramic package 10, as taught by Bates et al., is used for enclosing electronic devices, e.g., transistors, resistors, capacitors, and in particular integrated circuits. See Col. 1, lines 5-11. These type of ceramic packages are typically known in the Electronic Industry to be passive electronic components. In the Office Action, the Examiner misconstrued the teachings of the Bates et al. reference by indicating that the first layer or base layer 20 of ceramic material, is an integrated circuit. It was communicated to the Examiner during the phone interview on January 27, 2006, that the ceramic layer 20 is not an integrated circuit. Rather, an integrated circuit, as known in the Electronic Industry, is an active electronic circuit.

In view of the foregoing, the Bates reference does not anticipate independent Claim 15. Furthermore, since Claims 19, 20, and 24 are dependent claims that depend from independent Claim 15, it is also clear that the Bates reference does not, and cannot, anticipate dependent Claims 19, 20, and 24. Thus the rejection under 35 U.S.C. § 102(e), as being anticipated by Bates et al. should be overcome

Claim Rejections - 35 U.S.C. § 103

The Examiner rejected Claims 15-19 under 35 U.S.C. §103(a) as being unpatentable (obvious) over Moore (U.S. Patent No. 6,889,087) in view of Lin (U.S. Patent No. 6,511,865). The Examiner further rejected Claim 27 under 35 U.S.C. §103(a) as being unpatentable over Moore in view of Lin, and further in view of Kohno et al., (U.S. Patent No. 6,358,762).

Applicants respectfully traverse the rejections of Claims 15-19, and 27 in view of the Moore reference and the combined references of Moore, Lin, and Kohno et al. for the reasons set forth below. Moreover, as presently amended, Claim 15 includes an element which is not found or taught by Moore. The element *"creating a multi-layer surface on the top face of the integrated circuit"*, is not found or taught by Moore. Furthermore, the Examiner characterized Moore as failing to teach a process of creating a layer of insulation above at least some portions of the redistribution layer. For clarity purposes hereinafter, the redistribution layer, as described in Applicants' present application and as shown in FIGS. 6A and 6B, consists of one layer that make up the multi-layers created on the top face 207 of the integrated circuit. The insulation layer 714, also shown in FIGS. 6A consists of a top surface layer that covers the area that is not exposed by the interconnect pads 719 or the mounting pads 718. In the present application, Applicants further provide a process of creating the multi-layers, which process is descried in paragraphs **[0057]-[0069]**. As described in paragraph **[0069]**, this process "forms a custom-designed layout resulting in a number of pads 718 on which off-chip secondary components are directly mounted, as well as a number of test and interconnect pads 719/719A". Secondary components may be, e.g. capacitors, diodes, see paragraph **[0065]**. Such layers are not shown or taught by the Moore reference. All the Moore reference teaches is an electronic subassembly 300 which includes an integrated circuit 301, but it does not show or teach multi-layers created on the top face of the integrated circuit. The integrated circuit 301, shown and described in the Moore reference, may be a standard IC since Moore does not provide specifics for the design of the IC. A standard IC may also not provide the same benefits as the custom-design IC described in Applicants' present application. Thus, the subject matter as whole, as taught by the Moore reference, would not have been obvious at the time the invention was made to a person having ordinary skill in the art. The Moore reference falls short

of Applicants' invention because it lacks the process of making a custom IC having a multi-layer surface for mounting off-chip components.

As stated above, the Examiner characterized Moore as failing to teach a process of creating a layer of insulation above at least some portions of the redistribution layer. The Examiner further characterized Lin as teaching a process of making an electronic module including a process of providing an insulative adhesive layer between a chip and a circuit in order to provide mechanical attachment between the electronic components. The process of providing an insulative adhesive layer between a chip and a circuit, as taught by Lin, does not provide the same results as the layer of insulation described in Applicants' present application. Lin teaches using adhesive 140 as an electrical insulator for attaching support circuit 120 and chip 110, where the chip 110 is described as a semiconductor chip and the support circuit 120 is described as, e.g, a substrate. See FIGS. 1F, 3A, and 3B. Applicants teach creating a layer of insulation 714 above the redistribution layer 710, where the insulation layer consists of a top surface layer that covers the area that is not exposed by the interconnect pads 719 or the mounting pads 718.

Hence, it is respectfully submitted that a *prima facie* case of obviousness has not been established by the Moore reference alone, with the combination of the Moore and Lin references, or with the combination of the Moore, Lin, and Kohno references.

In view of the foregoing discussion, it is believed that the obviousness rejection is overcome with respect to independent Claim 15, and that this rejection should be withdrawn.

Claims 16-19 and 27 are dependent upon independent Claim 15 and, for this reason alone (although not necessarily the only reason) should be allowable for the same reasons that Claim 15 is allowable.

Conclusion

In view of the above, it is respectfully submitted that Claims 15-27 should be in condition for allowance. An indication of allowability with respect to these claims is earnestly solicited.

The Examiner is invited to telephone the undersigned, Victoria A. Poissant, should any issues remain after consideration and entry of this response, in order to permit early resolution of such issues.

Respectfully Submitted,

January 30, 2006

Victoria A. Poissant
Reg. No. 56,871

Attachments: Annotated Drawing Sheets showing changes to FIGS. 6A and 6B (2 pages);
Copy of Replacement Drawing Sheets (2 pages); and
Replacement Drawing Sheets (2 pages)

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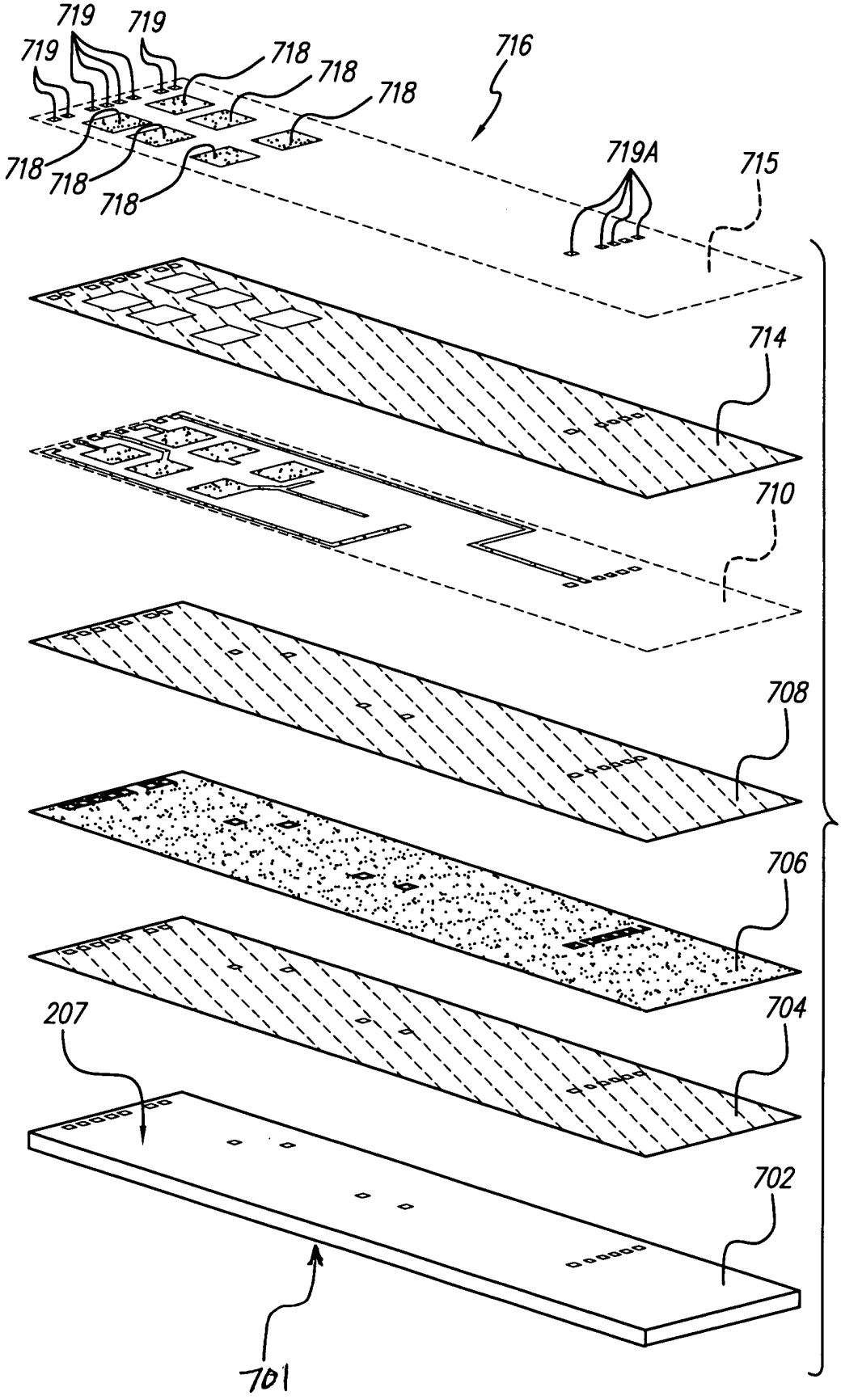

FIG. 6A

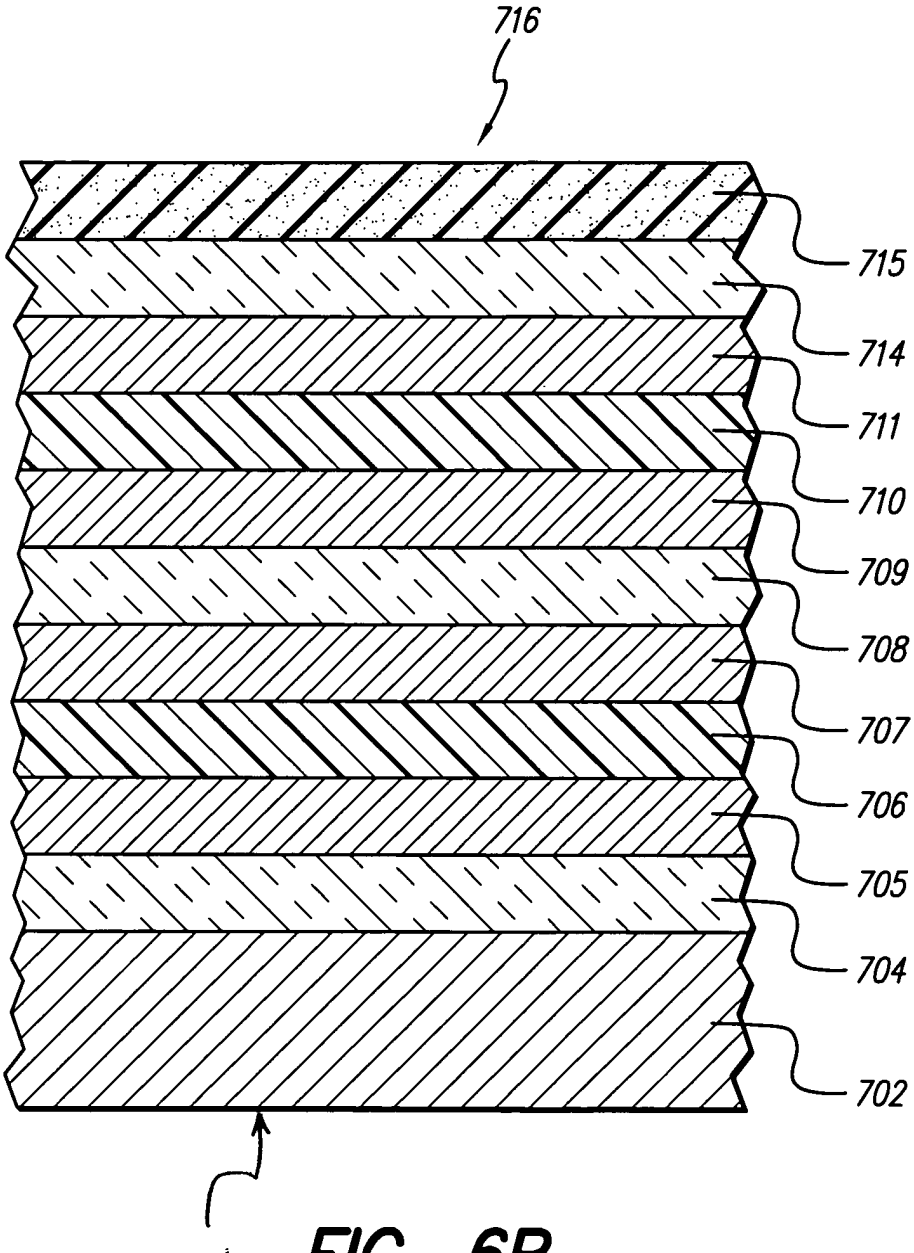

FIG. 6B